REMARKS/ARGUMENTS

Claims 1 - 4, 6 - 14, 17 - 20, and 23 are pending.

Claims 1 - 25 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Sun, U.S. Pat. No. 6,014,181 in view of Rodriquez et al., U.S. Patent No. 6,016,163.

The Present Invention

The present invention relates to motion detection using a DSP (digital signal processor). In accordance with the present invention as recited in claim 1, for example, a search window defining a sear area of data points is provided. A reference block is loaded into "a first memory portion." Then, a "first frame portion" which is "a subset of said search points" is loaded into "a second memory portion." A "first level search point" within the first frame portion is determined. Next, a "second frame portion" is then loaded into a third memory portion, being selected based on the first level search point. The memory portions are "portions of an on-chip memory of said DSP." Kindly see also independent claims 11 and 20.

The Reference to Sun

The reference to Sun describes a motion estimation algorithm. The Examiner cited Figs. 2 and 4 of Sun. These figures illustrate the principles of a conventional motion detection process. For example, Fig. 2 merely illustrates "the spatial relationship between the current macroblock in the current frame and search window in the previous frame (prior art)." *Col. 5, lines 19 - 21.* Fig. 2 does not show loading and searching a subset of the search window (the recited "first frame portion"), and then loading and searching a "second frame portion." In fact, Fig. 2 shows the entire "previous frame" and the entire "current frame."

Fig. 4 "is an example illustrating the last 3 steps in the step-search method of FIG. 3 (prior art)." *Col. 5, lines 25 - 26.* The figure is merely a pictorial representation of the processing of Fig. 3. A review of Fig. 3 does not reveal loading and performing a search in a "first frame portion" of a search window that is followed by loading and searching a "second frame portion" of the search window. Therefore, considered in the proper context of Fig. 3, the

elements in Fig. 4 likewise do not do not reveal loading and searching in a "first frame portion" followed by loading and searching in a "second frame portion."

The Reference to Rodriguez et al.

Rodriguez et al. were cited for showing the loading of first and second frame portions into the on-chip memory; in particular, column 5, lines 38 - 49. The cited portion however is merely a description of a conventional DSP configuration:

> "FIG. 2 shows a processor and memory system 201 which may be used to implement the invention. System 201 has a DSP 209 that has the above characteristics of the TMS320C80, a memory 203 which is divided into 32-bit words 205, and a 32-bit bus 207 which connects memory 203 and DSP 209. Beginning with memory 203, in memory 203, data is fetched along word boundaries 204; that is, the locations specified by addresses in memory 203 begin at word boundaries 204 and all reads are done on word boundaries. Word as used herein is thus to be understood as a unit of data which may be fetched from memory in a single operation."

The foregoing simply describes a system 201 that has a DSP 209. The system has a memory 203. The memory is divided into 32-bit words 205. There is a bus 207. Data is fetched on word boundaries. Respectfully, it is earnestly submitted that without more, the foregoing cited portion of Rodriguez et al. does not suggest loading a "first frame portion" to a portion of an on-chip memory, and then loading a "second frame portion" into a portion of the on-chip memory.

It is asserted in the Office action that "Rodriguez teaches that portions of the search windows can be stored and searched within the on board memory as required by the claims." *O.A., page 3.* As noted above the foregoing cited portion of Rodriguez et al. does not teach or suggest loading portions of the search window into an on-chip memory. Furthermore, a review of the Rodriguez et al. reference does not appear to reveal this aspect of the present invention.

As stated in column 4, lines 8 - 14, "[it] is an object of the present invention to provide improved techniques for comparing blocks of pixels which reduce the number of comparisons made in a block and which at the same time preserve vertical detail, are well adapted to use in the processor of a computer system, and can take advantage of whatever

parallel processing capabilities the processor may have." (underlining added). Rodriguez et al. disclose a comparison technique, not a search technique. Therefore, contrary to the assertion made in the Office action, Rodriguez et al. do not teach that portions of the search windows can be stored and searched within the on board memory as required by the claims.

"Video Processing is Memory Intensive"

As mentioned in the Office action, it is known that video processing requires large amounts of memory (see Rodriguez et al., col. 1, lines 23 - 25); "video processing is memory intensive." *O.A., page 3.* However, that fact in and of itself does not suggest the specific processing recited in the pending claims. Many solutions exist for addressing the fact that video processing requires large amounts of memory. The field of video compression techniques address the problem of large memory needs. The Sun reference teaches a video compression technique, but does not teach or recited the present invention as recited in the claims. Rodriguez et al. mention two methods in column 3, lines 32 - 50; however, Rodriguez et al. address "the computational cost of the block comparison itself." *Col. 3, lines 65 - 66.* They do not even address the issue of large memory requirements, instead Rodriguez et al. are concerned with improving the computational effort.

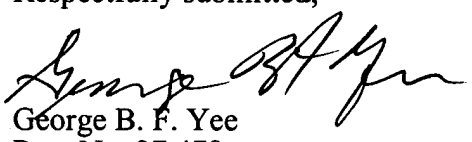
Based on the foregoing, there is no suggestion in the cited art to modify Sun to obtain the present invention. For at least any of the foregoing reasons, the Section 103 rejection of the claims, as amended, is believed to be overcome.

CONCLUSION

In view of the foregoing, all claims now pending in this Application are believed to be in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 650-326-2400.

Respectfully submitted,



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